Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte PABLO MARTIN RODRIGUEZ
and KENT R. TOWNLEY

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Appeal No. 2001-2660
Application 09/392,341

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ON BRIEF

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Before THOMAS, BARRETT, and BARRY, Administrative Patent Judges.

THOMAS, Administrative Patent Judge.

DECISION ON APPEAL

Appellants have appealed to the Board from the examiner's final rejection of claims 1, 2 and 4-13. Because the examiner has indicated at page 2 of the answer that two of the three rejections of the claims on appeal made under 35 U.S.C. § 103 have been withdrawn, including the rejection of claims 6 and 7, only claims 1, 2, 4, 5 and 8-13 remain for our consideration on appeal.

Representative claim 1 is reproduced below:

1. A switching circuit comprising:

a CMOS inverter having an input terminal coupled to a node, an output terminal, and comprising a nMOSFET;

a domino logic gate having an output terminal coupled to the node to drive the node HIGH and LOW;

a pullup pMOSFET having a gate at a logic level equal to the logic level of the CMOS inverter output terminal and having a drain coupled to the node to provide a half latch function to latch the node HIGH only when the node is brought HIGH; and

a bias circuit coupled to ground and to the CMOS inverter nMOSFET to increase the threshold voltage of the CMOS inverter nMOSFET compared to when its substrate and source are both at ground potential.

The following references are relied on by the examiner:

Magee 4,578,600 Mar. 25, 1986

Appellants' admitted prior art Figure 1

Claims 1, 2, 4, 5, and 8-13 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner relies upon appellants' admitted prior art Figure 1 in view of Magee.

Rather than repeat the positions of the appellants and the examiner, reference is made to the brief and the answer for the respective details thereof.

OPINION

As will be apparent from the following detailed discussion, we sustain only the rejection of independent claim 9 and reverse the rejection of the remaining claims on appeal.

From our study of the subject matter of independent claims 1, 4, 5, 8 and 9 on appeal in conjunction with appellants' admitted prior art, the teachings and suggestions of Magee and the examiner's reasoning of combinability, we do not sustain the rejection of independent claims 1, 4, 5 and 8.

From our detailed study of appellants' admitted prior art Figure 1 and the teachings and suggestions of Magee, we conclude that the artisan would have had no basis within 35 U.S.C. § 103 to have combined the teachings and suggestions of both of them. There appears to us to be no independent motivation other than the examiner's apparent reliance upon prohibited hindsight derived from appellants' claimed invention and the disclosed invention for the combination.

According to the description of prior art Figure 1 at specification page 2, it appears to be known in the art that undesirable crossbar currents and increased power dissipation exist in this circuit because the pMOSFET 160 of this figure does not turn off instantaneously. We are unconvinced that the

artisan necessarily would have found it obvious without more evidence to have employed the teaching value of Magee to have minimized or eliminated these prior art detrimental factors of the circuit of prior art Figure 1.

On the one hand, Magee emphasizes changing the bias voltage to make independent the threshold switching levels of the transistor circuit of his Figure 1, yet from the nature of the explanation of the operation and disadvantages of appellants' prior art Figure 1, there appears to be no relationship to the problems associated with appellants' prior art Figure 1 and the solution provided by Magee without first understanding the nature of the solution provided by appellants in the disclosed invention. The discussion on the disadvantages of appellants' admitted prior art Figure 1 does not indicate necessarily any problem with the threshold voltages of or bias voltages for any transistor of this figure such as to lead the artisan to the solution provided by Magee's Figure 1. Stated differently, the nature of the problems isolated by the discussion of the prior art in Magee does not appear to us to address or solve directly any of the known problems associated with appellants' prior art Figure 1.

Likewise, from our independent study of both references, we can derive no independent motivation from them for the combination. The examiner's reasoning of the combination at the top of page 4 of the examiner's answer of achieving benefits taught by Magee of eliminating the inherently mix-match of the switching between the individual field effect transistors in preventing erroneous operation of the half-latch of appellants' prior art Figure 1 appears to us to be more conclusory than to set forth a rationale within the art from the artisan to appreciate. Moreover, the examiner's additional rationale appears to recognize a certain identity of the structure of appellants' disclosed invention represented in Figure 2 and the latter portion of Magee's Figure 1, but this rationale indirectly reflects the apparent prohibited hindsight analysis of the examiner.

We also reverse the rejection of independent claims 1, 4, 5 and 8 on appeal for an additional reason. Each of these independent claims on appeal in part recites that the "CMOS" inverter comprise a "nMOSFET" transistor. The examiner's rationale at page 3 of the answer wrongly asserts that prior art Figure 1 shows a switching circuit comprising a CMOS inverter within the block element 110 comprising such an "nMOSFET"

transistor. Such is not shown in appellants' prior art Figure 1 and is not discussed at specification page 2 associated with this figure for the symbolic showing of the electrical inverter within the one-half latch circuit 110 in prior art Figure 1. There is no evidence before us that the symbolically shown inverter within the latch circuit 110 of prior art Figure 1 corresponds to the structure of a latch comprising a pMOSFET transistor 230 along with its corresponding nMOSFET transistor 220 as in appellants' disclosed Figure 2.

On the other hand, we sustain the rejection of independent claim 9 on appeal. In contrast to the other independent claims on appeal, this claim does not recite the CMOS inverter comprises an nMOSFET transistor as just discussed. In fact, the nature of the claimed domino gate and half-latch circuit in claim 9 is consistent from an artisan's perspective of the normal operation of appellants' prior art Figure 1 alone. As the examiner notes at the top of page 7 of the answer, the claimed first voltage corresponds to the input voltage applied to the domino gate 120 of appellants' prior art Figure 1 and the second voltage is the output voltage of the output node out according to the normal operation of the inverter circuit of this figure. In this sense

then the second voltage of appellants' claim may be greater than the claimed first voltage in appellants' prior art Figure 1.

Appellants' arguments at page 6 of the brief on appeal urging patentability of claim 9 are misplaced. The position set forth here as to this claim merely repeats the subject matter of claim 9 and makes no assertion that the references relied upon by the examiner does not meet the features and structure recited in this claim. We note that the claimed set of input voltages clearly is inclusive of a set of one to the extent shown in prior art Figure 1 such that the group of nMOSFETs 130 of the domino gate 120 may be one or a plurality of transistors.

We do not extend our affirmance of the rejection of claim 9 to its dependent claim 10 because claim 10 recites the same nMOSFET as a part of a CMOS inverter as recited in the other independent claims 1, 4, 5 and 8 as discussed earlier. The rejection of dependent claim 11 is also reversed because it depends from claim 10.

The examiner's rejection of claims 1, 2, 4, 5, and 8-13 under 35 U.S.C. § 103 is sustained only as to claim 9. Therefore, the decision of the examiner rejecting the claims on appeal under 35 U.S.C. § 103 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

James D. Thomas Administrative Patent Judge	)
Lee E. Barrett Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
Lance Leonard Barry Administrative Patent Judge	)

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